WHAT IS CLAIMED IS

1. A shared bus system, comprising:

a bus;

a first circuit which accesses said bus;

a second circuit which shares said bus with said first circuit, and accesses said bus;

a counter circuit which is provided in said second circuit, and performs a counting operation each time said second circuit accesses said bus; and

an arbiter circuit which arbitrates requests for a right to use said bus between said first circuit and said second circuit,

wherein said second circuit releases the right to use said bus in response to detection of a predetermined number of counting operations performed by said counter circuit after acquiring the right to use said bus from said arbiter circuit.

2. The shared bus system as claimed in claim 1, wherein said second circuit releases the right to use said bus when a required access operation comes to an end even before said counter circuit performs the predetermined number of counting operations.

3. The shared bus system as claimed in

claim 1, wherein said second circuit includes a register circuit, and the predetermined number is equal to a value stored in said register circuit.

4. The shared bus system as claimed in claim 3, wherein said second circuit includes:

a comparator which makes a comparison of a count indicated by said counter circuit with the value stored in said register circuit; and

a control circuit which notifies said arbiter circuit of the releasing of the right to use said bus according to the comparison by said comparator.

5. The shared bus system as claimed in claim 1, further comprising a second counter circuit which performs a counting operation each time a request for the right to use said bus is made to said arbiter circuit, and the predetermined number is a count indicated by said second counter circuit.

6. The shared bus system as claimed in claim 1, wherein said arbiter circuit disregards a request for the right to use said bus from said second circuit during a predetermined time period.

7. The shared bus system as claimed in claim 6, wherein said arbiter circuit includes a second counter circuit which performs a counting operation at predetermined intervals, and said predetermined time period is defined by a period during which a count indicated by said second counter circuit falls within a predetermined range.

8. The shared bus system as claimed in claim 1, wherein said bus is a memory bus to which a memory is connected, and said first circuit is a memory interface which accesses said memory through said memory bus.

9. The shared bus system as claimed in claim 1, wherein said second circuit is a liquid crystal display controlling circuit which controls driving of a liquid crystal display device through said memory bus.

10. A method of sharing a bus, comprising the steps of:

acquiring a right to use a shared bus by making a request;

counting a number of accesses made to the shared bus after acquiring the right to use the shared bus; and

releasing the shared bus in response to an event that the number of accesses reaches a predetermined number.

11. The method as claimed in claim 10, further comprising a step of releasing the right to use said shared bus when a required access operation comes to an end even before the number of accesses reaches the predetermined number.

12. The method as claimed in claim 10, further comprising a step of storing a value in a register circuit, and the predetermined number is equal to the value stored in said register circuit.

13. The method as claimed in claim 12, further comprising the steps of:

making a comparison of the counted number with the value stored in said register circuit; and

notifying an arbiter circuit of the releasing of the right to use said shared bus according to the comparison.

14. The method as claimed in claim 10, further comprising a step of performing a counting

operation each time a request for the right to use said shared bus is made, and the predetermined number is a count indicated by the counting operation.

15. The method as claimed in claim 10, further comprising a step of disregarding a request for the right to use said shared bus during a predetermined time period.

16. The method as claimed in claim 15, further comprising a step of performing a counting operation at predetermined intervals, and said predetermined time period is defined by a period during which a count indicated by said counting operation falls within a predetermined range.

17. The method as claimed in claim 10, wherein said bus is a memory bus to which a memory is connected, and a memory interface for accessing said memory through said memory bus shares said memory bus together with a liquid crystal display controlling circuit for controlling driving of a liquid crystal display device through said memory bus.